STIC EIC 2100 Search Request Form

133060
90

Today's Date: 9/20/04

What date would you like to use to limit the search?
Priority Date:
Other:

Name Brian R. Peko

AU 2187 Examiner # 77024

Room # 2C04 Phone 306-5843

Serial # 10/628,434

Format for Search Results (Circle One):
PAPER DISK EMAIL

Where have you searched so far?
USP DWPI EPO JPO ACM IBM TDB
IEEE INSPEC SPI Other

Is this a "Fast & Focused" Search Request? (Circle One) YES NO
A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Request History Buffer

If No Flag : See Fig. 3C

. Flag, bit, indicator

. Claims 1 + 17 most pertinent

. Stride : value used to increase/decrease orginal Address value
→ 2nd mem location based on 1st mem location
(stride = 2 in Fig. 3C)

Add Flag + stride

IC Searcher _____ Phone _____

te picked up _____ Date Completed _____

Search and Information Resources Administration

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File   2:INSPEC 1969-2004/Sep W3
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Sep W3
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Sep W3
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Sep W3
         (c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Aug
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Sep W4
         (c) 2004 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2004/Aug W5
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Aug
         (c) 2004 The HW Wilson Co.
File 144:Pascal 1973-2004/Sep W3
         (c) 2004 INIST/CNRS

Set     Items   Description
S1         66   AU=(HUM H? OR HUM, H? OR BOGIN Z? OR BOGIN, Z?)
S2          0   S1 AND HISTOR??(3N)(BUFFER?? OR CACHE?? OR TEMPORARY??(2N)-
              STORAG???)
S3          0   S2 AND (FLAG?? OR BIT OR BITS OR INDICATOR?? )
S4          0   S1 AND (PRE()(FETCH??? OR READ??? OR LOAD???) OR PREFETCH?-
              ?? OR PRELOAD??? OR PREREAD???)
S5          0   S1 AND ((SECOND??? OR 2ND?? OR NEXT?? OR SUBSEQUENT???)(4N-
              )(MEMOR???? OR STORAGE??? OR RAM? ?)(2N)(LOCATION?? OR ADDRES-
              S??))
S6          0   S5 NOT S2
S7          0   S4 AND STRID?
```

```
File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
File 347:JAPIO Nov 1976-2004/May(Updated 040903)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Sep W02
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040923,UT=20040916
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200461
         (c) 2004  Thomson Derwent

Set     Items   Description
S1         82   AU=(HUM H? OR HUM, H? OR BOGIN Z? OR BOGIN, Z?)
S2          2   S1 AND HISTOR??(3N)(BUFFER?? OR CACHE?? OR TEMPORARY??(2N)-
              STORAG???)
S3          2   S2 AND (FLAG?? OR BIT OR BITS OR INDICATOR?? )
S4         10   S1 AND (PRE()(FETCH??? OR READ??? OR LOAD???) OR PREFETCH?-
              ?? OR PRELOAD??? OR PREREAD???)
S5          1   S1 AND ((SECOND??? OR 2ND?? OR NEXT?? OR SUBSEQUENT???)(4N-
              )(MEMOR???? OR STORAGE??? OR RAM? ?)(2N)(LOCATION?? OR ADDRES-
              S??))
S6          1   S5 NOT S2
S7          0   S4 AND STRID?
```

3/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

016169895 **Image available**
WPI Acc No: 2004-327782/200430
Related WPI Acc No: 2003-874452
XRPX Acc No: N04-261484
Computer system has pre-fetcher which pre-fetches data associated with specified memory location from memory, if no flag **associated with specified memory location is in request** history buffer
Patent Assignee: BOGIN Z (BOGI-I); HUM H H (HUMH-I)
Inventor: **BOGIN Z ; HUM H H**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040059873	A1	20040325	US 2000541392	A	20000331	200430	B
			US 2003628434	A	20030729		

Priority Applications (No Type Date): US 2000541392 A 20000331; US 2003628434 A 20030729
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040059873	A1		21	G06F-012/08	Cont of application US 2000541392 Cont of patent US 6643743

... **pre-fetcher which pre-fetches data associated with specified memory location from memory, if no** flag **associated with specified memory location is in request** history buffer
Inventor: **BOGIN Z** ...

... **HUM H H**

Abstract (Basic):
... A prefetch control unit checks the request **history buffer** (RHB) for **flag** associated with specified memory location that is based on previous memory location called by processor...

...pre-fetcher pre-fetches data associated with the specified memory location from memory, if no **flag** associated with the specified memory location is in the RHB.
...Title Terms: **FLAG ;**

3/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

015812248 **Image available**
WPI Acc No: 2003-874452/200381
Related WPI Acc No: 2004-327782
XRPX Acc No: N03-698165
Data prefetching method in cache, involves storing flag **in response to fetching of data from memory, in request** history buffer **for further data access**
Patent Assignee: INTEL CORP (ITLC)
Inventor: **BOGIN Z ; HUM H H**
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6643743	B1	20031104	US 2000541392	A	20000331	200381 B

Priority Applications (No Type Date): US 2000541392 A 20000331

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6643743	B1		12	G06F-012/00	

Data prefetching method in cache, involves storing flag **in response to fetching of data from memory, in request** history buffer **for further data access**

Inventor: **BOGIN Z** ...

... **HUM H H**

Abstract (Basic):

... involves fetching data from a memory according to a request from a memory address. A **flag** is stored in response to fetching process, in a request **history buffer** (RHB) (8). Another data is prefetched from another memory address, when data from the another...

... request **history buffer** (8...

...Title Terms: **FLAG** ;

6/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015354840 **Image available**
WPI Acc No: 2003-415778/200339
XRPX Acc No: N03-331290

Memory controller subsystem for computer system, has read request controller which receives read request from processor or input output devices to control dispatching of prefetch requests to main memory

Patent Assignee: INTEL CORP (ITLC)
Inventor: **BOGIN Z** ; CLOHSET S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6523093	B1	20030218	US 2000675893	A	20000929	200339	B

Priority Applications (No Type Date): US 2000675893 A 20000929
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6523093	B1		11	G06F-012/00	

Inventor: **BOGIN Z** ...

Abstract (Basic):
... request is read from the processor, corresponding data is returned to the processor and the **next** sequential **address** is prefetched from the **memory** , thus once the processor starts a stream of read requests in an incrementing fashion, the...

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File 348:EUROPEAN PATENTS 1978-2004/Sep W02
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040923,UT=20040916
         (c) 2004 WIPO/Univentio

Set     Items   Description
S1        507   HISTOR??(3N)(BUFFER?? OR CACHE?? OR TEMPORARY??(2N)STORAG?-
                ??)
S2     264192   FLAG?? OR BIT OR BITS OR INDICATOR??
S3      44491   (MEMOR???? OR STORAGE??? OR RAM? ?)(2N)(LOCATION?? OR ADDR-
                ESS??)
S4       5794   (SECOND??? OR 2ND?? OR NEXT?? OR SUBSEQUENT???)(4N)S3
S5      20912   (PRE()(FETCH??? OR READ??? OR LOAD???) OR PREFETCH??? OR P-
                RELOAD??? OR PREREAD???)
S6       2408   STRIDE??? OR STRIDING??
S7     726771   INTERVAL?? OR GAP?? OR DISTANC??
S8          2   S1(S)S4
S9         38   S1(S)S3
S10         5   S9(S)S5
S11         5   S10 NOT S8
S12         4   S11(S)S2
S13         2   S12 NOT (CARTRIDGE?)
S14         0   S9(3N)S6
S15         1   S9(3N)S7
```

8/3,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00984064 **Image available**

A PRINTING CARTRIDGE WITH SWITCH ARRAY IDENTIFICATION

CARTOUCHE D'IMPRESSION AVEC IDENTIFICATION D'UNE MATRICE DE COMMUTATEURS

Patent Applicant/Assignee:
SILVERBROOK RESEARCH PTY LTD, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
SILVERBROOK Kia, Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU, AU (Residence), AU (Nationality), (Designated only for: US)
Legal Representative:
SILVERBROOK Kia (agent), Silverbrook Research Pty Ltd, 393 Darling Street, Balmain, New South Wales 2041, AU,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200313860 A1 20030220 (WO 0313860)
Application: WO 2002AU1053 20020806 (PCT/WO AU0201053)
Priority Application: US 2001922029 20010806
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI
SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 142964

Fulltext Availability:
Detailed Description

Detailed Description

... s point in the same strip, so it can be kept in a 32-entry **history buffer** . The basic of the calculate span process are as illustrated in Fig. 88 with the...B ABS(Ply - POY)
Store Ply in POY history
7 A = MAX(A, B)
The **history buffers** 365, 366 are cached DRAM. The 'Previous Line' (for P2 **history**) **buffer** 366 is 32 entries of span-precision. The 'Previous Point' (for PO **history**). **Buffer** 365 requires I register that is used most of the time (for calculation of points I to 31 of a line in a strip), and a DRAM **buffered** set of **history** values to be used in the calculation of point 0 in a strip's line.

32 bit precision in span **history** requires 4 **cache** lines to hold P2 history, and 2 for PO history. PO's history is only...image. The first stage requires the Address Unit and a single Adder ALU, with the **address** of the histogram table 377 for initialising.

Relative Microcode **Address** Unit Adder Unit 1
Address A = Base address of histogram
0 Write 0 to Outl = A
A + (Adderl.Outl << 2...

8/3,K/2 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00566564 **Image available**
COMPUTER SYSTEM, COMPUTER-READABLE STORAGE MEDIUM AND METHOD OF OPERATING SAME, AND METHOD OF OPERATING THAT SYSTEM
SYSTEME INFORMATIQUE, SUPPORT DE STOCKAGE LISIBLE PAR ORDINATEUR, PROCEDE DE FONCTIONNEMENT ET PROCEDE DE MISE EN SERVICE DUDIT SYSTEME

Patent Applicant/Assignee:
INSIGNIA SOLUTIONS PLC, Insignia House, The Mercury Centre, Wycombe Lane, Wooburn Green, High Wycombe, Buckinghamshire HP10 0HH, GB, GB (Residence), GB (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
PLUMMER Wayne, 6 Sunningdale Close, Booker, High Wycombe, Bucks. HP12 4EN , GB, GB (Residence), GB (Nationality), (Designated only for: US)
CHARNELL William Thomas, Bereton, Nags Head Lane, Great Missenden HP16 0HG, GB, GB (Residence), GB (Nationality), (Designated only for: US)
DARNELL Stephen, 45 Heynes Green, Maidenhead, Berks. SL6 3NA, GB, GB (Residence), GB (Nationality), (Designated only for: US)
DIAS Blaise Abel Alec, 7 North Way, Uxbridge, Middx. UB10 GNG, GB, GB (Residence), GB (Nationality), (Designated only for: US)
GUTHRIE Philippa Joy, 5 Manor Farm Court, Hardwick, Aylesbury, Bucks. HP22 4DH, GB, GB (Residence), GB (Nationality), (Designated only for: US)
KRAMSKOY Jeremy Paul, 12 Claremont Terrace, Portsmouth Road, Long Ditton, Surrey KT7 0XP, GB, GB (Residence), GB (Nationality), (Designated only for: US)
SEXTON Jeremy James, 164 Great Elms Road, Bennetts End, Hemel Hempstead, Herts. HP3 9UQ, GB, GB (Residence), GB (Nationality), (Designated only for: US)
WYNN Michael John, 11 North Town Road, Maidenhead, Berks. SL6 7TQ, GB, GB (Residence), GB (Nationality), (Designated only for: US)
RAUTENBACH Keith, 180 Kingsmead Road, High Wycombe, Bucks. HP11 1JL, GB, GB (Residence), GB (Nationality), (Designated only for: US)
THOMAS Stephen Paul, 16 Lansdowne Way, High Wycombe, Bucks. HP11 1TR, GB, GB (Residence), GB (Nationality), (Designated only for: US)
Legal Representative:
COZENS Paul Dennis (et al) (agent), Mathys & Squire, 100 Grays Inn Road, London WC1X 8AL, GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200029937 A2 20000525 (WO 0029937)
Application: WO 99GB788 19990316 (PCT/WO GB9900788)
Priority Application: GB 9825102 19981116
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW SD SL SZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 81643

Fulltext Availability:
Detailed Description

Detailed Description
... as well as recording how many times a particular block has been interpreted, the execution **history** recorder also records further information regarding the execution of the block, for example, from where ...onto 1 5 registers for the compiled version has to be restored into the correct **memory location** before the **next** section of code is generated. Thus the return handling glue code restores any states which ...
?

13/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00934731
Combined branch prediction and cache prefetch in a microprocessor
Kombinierte Sprungvorhersage und Cachevorauslade in einem Prozessor
Prediction de branchement et preextraction d'antememoire combinee dans un processeur

PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279074), P.O. Box 655474, 13500 Central Expressway, Dallas, TX 75265, (US), (Applicant designated States: all)
INVENTOR:
Shiell, Jonathan H., 4300 Longfellow Dr., Plano, TX 75093, (US)
Bondi, James O., 4317 Brady Dr., Plano, TX 75024, (US)
LEGAL REPRESENTATIVE:
Harris, Ian Richard (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 851344 A2 980701 (Basic)
EP 851344 A3 000119
APPLICATION (CC, No, Date): EP 97310548 971223;
PRIORITY (CC, No, Date): US 33435 P 961223
DESIGNATED STATES: DE; FR; GB; IT; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-009/38
ABSTRACT WORD COUNT: 143
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9827	1589
SPEC A	(English)	9827	12202
Total word count - document A			13791
Total word count - document B			0
Total word count - documents A + B			13791

...SPECIFICATION includes prefetch address portions PF0 ADDR, PF1 ADDR that store the memory addresses to be **prefetched** . In addition, according to this embodiment of the invention, entry 63i)) also includes **prefetch** counters PF0 CTR, PF1 CTR, which are associated with the **prefetches** PF0, PF1, respectively. **Prefetch** counters PF0 CTR, PF1 CTR are small counters, such as two- **bit** counters, that maintain information regarding the results of the **prefetch** ; of course, **prefetch** counters PF0 CTR, PF1 CTR may be larger counters if further granularity in the **cache history** of the **prefetches** is desired. In this embodiment of the invention, **prefetch** counters PF0 CTR, PF1 CTR are each incremented in response to their associated **prefetch** being a level 2 cache miss and thus requiring access to main memory 305. Conversely, **prefetch** counters PF0 CTR, PF1 CTR are decremented each time that the associated **prefetch** is unnecessary, as the sought-for data or instructions are already in cache; upon a **prefetch** counter PF0 CTR, PF1 CTR reaching zero, its control **bits** PF0C, PF1C in **prefetch** control portion PF CTL are set to the invalid state (00), permitting a new **prefetch** to be set up therein.

As noted in the above description, entry 63i)) includes the...

13/3,K/2 **(Item 2 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00306062
Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme du traitement de donnees numeriques.
PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Gruner, Ronald Hans, 112 Dublin Wood Drive, Cary North Carolina 27514, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Schleimer, Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514, (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)
LEGAL REPRESENTATIVE:
Robson, Aidan John et al (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 300516 A2 890125 (Basic)
EP 300516 A3 890426
EP 300516 B1 931124
APPLICATION (CC, No, Date): EP 88200921 820521;
PRIORITY (CC, No, Date): US 266413 810522; US 266539 810522; US 266521 810522; US 266415 810522; US 266409 810522; US 266424 810522; US 266421 810522; US 266404 810522; US 266414 810522; US 266532 810522; US 266403 810522; US 266408 810522; US 266401 810522; US 266524 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556 (EP 823025960)
INTERNATIONAL PATENT CLASS: G06F-009/46; G06F-012/14;
ABSTRACT WORD COUNT: 122

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1018
CLAIMS B	(German)	EPBBF1	868
CLAIMS B	(French)	EPBBF1	1115
SPEC B	(English)	EPBBF1	154256
Total word count - document A			0
Total word count - document B			157257
Total word count - documents A + B			157257

...SPECIFICATION previously described, Addressing Mechanisms 10220 comprise UID/AON Tables 10222, Memory Management Tables 10224, Name **Cache** 10226, and Address Translation Unit 10228.
UID/AON Tables 10222 relate each object's UID...

15/3,K/1 **(Item 1 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

01538576
Network usage analysis system and method for updating statistical models
System und Verfahren zur Analyse der Auslastung von Netzwerken mit Aktualisierung statistischer Modelle
Systeme et procede d'analyse d'utilisation d'un reseau, comportant l'actualisation de modeles statistiques
PATENT ASSIGNEE:
Hewlett-Packard Company, (206037), 3000 Hanover Street, Palo Alto, CA 94304, (US), (Applicant designated States: all)
INVENTOR:
Rhodes, N. Lee, 1165 Diamond Court, Los Altos, CA 94024, (US)
LEGAL REPRESENTATIVE:
Tollett, Ian et al (86293), Williams Powell 4 St. Paul's Churchyard, London EC4M 8AY, (GB)
PATENT (CC, No, Kind, Date): EP 1282269 A1 030205 (Basic)
APPLICATION (CC, No, Date): EP 2002255294 020730;
PRIORITY (CC, No, Date): US 919527 010731
DESIGNATED STATES: DE; GB; IT
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04L-012/26; H04L-012/24
ABSTRACT WORD COUNT: 68
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200306	611
SPEC A	(English)	200306	6997
Total word count - document A			7608
Total word count - document B			0
Total word count - documents A + B			7608

...SPECIFICATION the time interval over which the statistical data is collected to be a rolling time **interval** . **History cache** 24 is used for organizing and storing statistical data over a rolling time interval, i...minutes), wherein each memory array segment is associated with a corresponding 5 minute update time **interval** 210. **Memory address** 212 illustrates the beginning memory address for each memory array segment 206.
Record events or...

```
File   8:Ei Compendex(R) 1970-2004/Sep W3
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Aug
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/Sep 09
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Sep W4
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Sep W3
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/Aug W5
         (c)2004 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/Sep 27
         (c) 2004 The Gale Group
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File   6:NTIS 1964-2004/Sep W3
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/Sep W3
         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Sep W3
         (c) 2004 Inst for Sci Info
File  62:SPIN(R) 1975-2004/Jul W4
         (c) 2004 American Institute of Physics
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Aug
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK

Set     Items   Description
S1        219   HISTOR??(3N)(BUFFER?? OR CACHE?? OR TEMPORARY??(2N)STORAG?-
                ??)
S2     638601   FLAG?? OR BIT OR BITS OR INDICATOR??
S3       9870   (MEMOR???? OR STORAGE??? OR RAM? ?)(2N)(LOCATION?? OR ADDR-
                ESS??)
S4        119   (SECOND??? OR 2ND?? OR NEXT?? OR SUBSEQUENT???)(4N)S3
S5      22326   (PRE()(FETCH??? OR READ??? OR LOAD???) OR PREFETCH??? OR P-
                RELOAD??? OR PREREAD???)
S6      11591   STRIDE??? OR STRIDING??
S7    2174630   INTERVAL?? OR GAP?? OR DISTANC??
S8         12   S1 AND S2
S9          0   S8 AND S4
S10         0   S1 AND S4
S11         4   S1 AND S3
S12         0   S11 AND S2
S13         0   S11 AND S5
S14         2   S1 AND S6
S15        18   S1 AND S7
S16         0   S15 AND S3
S17         1   RD S14 (unique items)
S18         3   RD S11 (unique items)
S19        25   S1 AND S5
S20        13   RD (unique items)
S21        12   S20 NOT (S11 OR S14)
S22         0   S21 AND S8
```

17/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06864288 E.I. No: EIP04228179049
Title: Data cache prefetching using a global history buffer
Author: Nesbit, Kyle J.; Smith, James E.
Corporate Source: Department of Electrical Engineering University of Wisconsin, Madison, WI, United States
Conference Title: Proceedings - 10th International Symposium on High Performance Computer Architecture
Conference Location: Madrid, Spain Conference Date: 20040214-20040218
Sponsor: IEEE Computer Society,TCCA; Institute of Electrical and Electronics Engineers (IEEE); IEEE Computer Society; Intel; et al
E.I. Conference No.: 62888
Source: IEEE High-Performance Computer Architecture Symposium Proceedings Proceedings - 10th International Symposium on High Performance Computer Architecture v 10 2004.
Publication Year: 2004
CODEN: 85QSAT ISSN: 1530-0897
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0406W1
Abstract: A new structure for implementing data cache prefetching is proposed and analyzed via simulation. The structure is based on a Global **History Buffer** that holds the most recent miss addresses in FIFO order. Linked lists within this global **history buffer** connect addresses that have some common property, e.g. they were all generated by the same load instruction. The Global **History Buffer** can be used for implementing a number of previously proposed prefetch methods, as well as new ones. Prefetching with the Global **History Buffer** has two significant advantages over conventional table prefetching methods. First, the use of a FIFO **history buffer** can improve the accuracy of correlation prefetching by eliminating stale data from the table. Second, the Global **History Buffer** contains a more complete (and intact) picture of **cache** miss **history**, creating opportunities to design more effective prefetching methods. Global **History Buffer** prefetching can increase correlation prefetching performance by 20% and cut its memory traffic by 90%. Furthermore, the Global **History Buffer** can make correlations within a load's address stream, which can increase **stride** prefetching performance by 5%. Collectively, the Global **History Buffer** prefetching methods perform as well or better than the conventional prefetching methods studied on 14 of 15 benchmarks. 17 Refs.
Descriptors: *Microprocessor chips; Cache memory; Computer architecture; Benchmarking; Clocks; Correlation methods; Computer simulation
Identifiers: Prefetching; Global **history buffer** (GHB); **Cache** miss
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 722.1 (Data Storage, Equipment & Techniques); 943.3 (Special Purpose Instruments); 922.2 (Mathematical Statistics); 723.5 (Computer Applications)
714 (Electronic Components & Tubes); 722 (Computer Hardware); 912 (Industrial Engineering & Management); 943 (Mechanical & Miscellaneous Measuring Instruments); 922 (Statistical Methods); 723 (Computer Software, Data Handling & Applications)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT); 94 (INSTRUMENTS & MEASUREMENT); 92 (ENGINEERING MATHEMATICS)
?

18/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01483073 E.I. Monthly No: EI8401001391 E.I. Yearly No: EI84022571
Title: CACHE **MISS** HISTORY **TABLE**.
Author: Rechtschaffen, R. N.
Source: IBM Technical Disclosure Bulletin v 25 n 11B Apr 1983 p 5978-5980
Publication Year: 1983
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH
Journal Announcement: 8401
Abstract: In a model of program behavior involving re-entrant code, the re-execution of a code segment will recreate cache accesses if the contents of the base registers are the same. It has been found that there is a high degree of register reuse and that the **memory address** can serve as a surrogate for the contents of the registers. These results lead one to suspect that the cache can predict accesses accurately based only on the sequence of cache accesses. It is proposed to capture information about miss patterns and use that information to prestage cache lines, thereby reducing the penalty associated with a cache miss. The processor maintains the **history** of **cache** misses by building and updating a **cache** miss **history** table.
Descriptors: *COMPUTER OPERATING SYSTEMS
Classification Codes:
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

18/5/2 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

4554405 INSPEC Abstract Number: A9403-2920-001, B9402-7410B-011, C9402-5520-001
Title: Preliminary design of the BPM electronics memory scanner for the Advanced Photon Source
Author(s): Votaw, A.J.
Author Affiliation: Argonne Nat. Lab., IL, USA
Journal: AIP Conference Proceedings no.281 p.242-7
Publication Date: 1993 Country of Publication: USA
CODEN: APCPCS ISSN: 0094-243X
U.S. Copyright Clearance Center Code: 0094-243X/93/$2.00
Conference Title: Fourth Annual Workshop on Accelerator Instrumentation
Conference Date: 27-30 Oct. 1992 Conference Location: Berkeley, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: The memory scanner is a VXI module that is part of the Advanced Photon Source (APS) beam position monitor (BPM) data acquisition system. Each module is designed to gather and process digital data from up to nine digital channels transmitting the BPM data from the **storage** ring (360 **locations**) and the synchrotron (80 locations). It stores beam **history** in a **buffer** , performs a running average of the X and Y position data, stores the latest scan of all channels, and provides high speed digital output of the beam position data for the global orbit feedback system. The system's capability to support single pass, closed orbit, and tune

measurement functions will also be briefly described. (3 Refs)
Subfile: A B C
Descriptors: data acquisition; electron accelerators; particle beam diagnostics; physics computing; signal processing equipment; storage rings
Identifiers: closed orbit measurement; single pass measurement; memory scanner; VXI module; Advanced Photon Source; data acquisition system; global orbit feedback system; tune measurement
Class Codes: A2920D (Storage rings); A0650D (Data gathering, processing, and recording, data displays including digital techniques); B7410B (Beam handling and diagnostics); B7210G (Data acquisition systems); B7220 (Signal processing and conditioning equipment and techniques); C5520 (Data acquisition equipment and techniques); C7320 (Physics and Chemistry); C5260 (Digital signal processing)

18/5/3 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1729133 NTIS Accession Number: DE93007893
Preliminary design of the BPM electronics memory scanner/dual boxcar averager for the Advanced Photon Source
Votaw, A. J.
Argonne National Lab., IL.
Corp. Source Codes: 001960000; 0448000
Sponsor: Department of Energy, Washington, DC.
Report No.: ANL/ASD/CP-77461; CONF-9210246-17
1992 8p
Languages: English Document Type: Conference proceeding
Journal Announcement: GRAI9315; ERA9329
1992 accelerator instrumentation workshop, Berkeley, CA (United States), 27-30 Oct 1992. Sponsored by Department of Energy, Washington, DC.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Country of Publication: United States
Contract No.: W-31109-ENG-38
The memory scanner/dual boxcar averager are VXI modules that are part of the Advanced Photon Source (APS) beam position monitor (BPM) data acquisition system. Each pair of modules is designed to gather and process digital data from up to nine digital channels transmitting the BPM data from the **storage** ring (360 **locations**) and the synchrotron (80 locations). They store beam **history** in a **buffer** , store the latest scan of all channels, and provide boxcar averaged X and Y position data for the global orbit feedback system, provide boxcar average X and Y position data for beam diagnostics, and a buffered output of SCDU data as it is scanned for the beam abort interlock system. The system's capability to support single pass, closed orbit and tune measurement functions will also be briefly described.
Descriptors: *Beam Monitors; *Advanced Photon Source; Beam Position; Data Acquisition Systems; Design; Electronic Equipment; Feedback
Identifiers: EDB/430303; NTISDE
Section Headings: 46GE (Physics--General)

21/3,K/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06868222 E.I. No: EIP04228186622
Title: Call graph prefetching **for database applications**
Author: Annavaram, Murali; Patel, Jignesh M.; Davidson, Edward S.
Corporate Source: Intel Corporation, Santa Clara, CA 95052-8119, United States
Source: ACM Transactions on Computer Systems v 21 n 4 November 2003. p 412-444
Publication Year: 2003
CODEN: ACSYEC ISSN: 0734-2071
Language: English

Title: Call graph prefetching **for database applications**
...Abstract: and hence do not use processor caches effectively. In this paper, we propose Call Graph **Prefetching** (CGP), an N instruction **prefetching** technique that analyzes the call graph of a database system and **prefetches** instructions from the function that is deemed likely to be called next. CGP capitalizes on...

...and uses the predictable call sequences in the call graph to determine which function to **prefetch** next. The hardware-based CGP(CGP...
...H) uses a hardware table, called the Call Graph **History Cache** (CGHC), to dynamically store sequences of functions invoked during program execution, and uses that stored history when choosing which functions to **prefetch** . We evaluate the performance of CGP on sets of Wisconsin and TPC-H queries, as...

...applications the number of instruction cache (I-cache) misses were very few even without any **prefetching** , obviating the need for CGP. On the other hand, the database workloads do suffer a...
Identifiers: Instruction cache **prefetching** ; Call graph; Database

21/3,K/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05982348 E.I. No: EIP01566811788
Title: The potential costs and benefits of long-term prefetching **for content distribution**
Author: Venkataramani, A.; Yalagandula, P.; Kokku, R.; Sharif, S.; Dahlin, M.
Corporate Source: Department of Computer Sciences University of Texas, Austin, TX 78712, United States
Source: Computer Communications v 25 n 4 Mar 1 2002. p 367-375
Publication Year: 2002
CODEN: COCOD7 ISSN: 0140-3664
Language: English

Title: The potential costs and benefits of long-term prefetching **for content distribution**
Abstract: This paper examines the costs and potential benefits of long-term **prefetching** for content distribution. In traditional short-term **prefetching** , **caches** use recent access **history** to predict and **prefetch** objects likely to be referenced in the near future. In

contrast, long-term **prefetching** uses long-term steady state object access rates and update frequencies to identify objects to replicate to content distribution locations. Compared to demand caching, long-term **prefetching** increases network bandwidth and disk space costs but may benefit a system by improving hit...

...analytic models and trace-based simulations, we examine algorithms for selecting objects for long-term **prefetching** . We find that although the Zipf-like popularity distribution of web objects makes it challenging to **prefetch** enough objects to significantly improve hit rates, systems can achieve significant benefits at modest costs...

21/3,K/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04962631 E.I. No: EIP98034097253
Title: Prediction caches for superscalar processors
Author: Bennett, James E.; Flynn, Michael J.
Corporate Source: Stanford Univ, Stanford, CA, USA
Conference Title: Proceedings of the 1997 30th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-30
Conference Location: Triangle Park, NC, USA Conference Date: 19971201-19971203
E.I. Conference No.: 48027
Source: Proceedings of the Annual International Symposium on Microarchitecture 1997. IEEE Comp Soc, Los Alamitos, CA, USA,97TB100184. p 81-90
Publication Year: 1997
CODEN: PSMIE7 ISSN: 1072-4451
Language: English

...Abstract: present in the cache. However, memory latency still affects performance in the case of a **cache** miss. Prediction **caches** use a **history** of recent **cache** misses to predict future misses and to reduce the overall cache miss rate. This paper...
...prediction caches, and introduces a new kind of prediction cache, which combines the features of **prefetching** and victim caching. This new cache is shown to be more effective at reducing miss...

21/3,K/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04862208 E.I. No: EIP97103902715
Title: Using speculative retirement and larger instruction windows to narrow the performance gap between memory consistency models
Author: Ranganathan, Parthasarathy; Pai, Vijay S.; Adve, Sarita V.
Corporate Source: Rice Univ, Houston, TX, USA
Conference Title: Proceedings of the 1997 9th Annual ACM Symposium on Parallel Algorithms and Architectures, SPAA
Conference Location: Newport, RI, USA Conference Date: 19970622-19970625
E.I. Conference No.: 47176
Source: Annual ACM Symposium on Parallel Algorithms and Architectures 1997. ACM, New York, NY, USA. p 199-210

Publication Year: 1997
CODEN: AASAES
Language: English

...Abstract: the impact o.f current hardware optimizations to memory consistency implementations, hardware-controlled non-binding **prefetching** and speculative load execution, on the performance of the processor consistency (PC) memory model. We...
...over PC in some cases, because PC suffers from the negative effects of premature store **prefetches** and insufficient memory queue sizes. The second part of the paper proposes and evaluates a...

...previous store is outstanding. Speculative retirement needs additional hardware support (in the form of a **history buffer**) to recover from possible consistency violations due to such speculative retires. With a 64 element **history buffer** , speculative retirement reduces the execution time gap between SC and PC to within 11% for...

21/3,K/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04602175 E.I. No: EIP97013495447
Title: Design decisions influencing the ultraSPARC's instruction fetch architecture
Author: Yung, Robert
Corporate Source: Sun Microsystems Inc
Conference Title: Proceedings of the 1996 29th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-29
Conference Location: Paris, Fr Conference Date: 19961202-19961204
E.I. Conference No.: 45848
Source: Proceedings of the Annual International Symposium on Microarchitecture 1996. IEEE, Los Alamitos, CA, USA,96TB100075. p 178-190
Publication Year: 1996
CODEN: PSMIE7 ISSN: 1072-4451
Language: English

...Abstract: instruction issue rate and must predict future instruction sequences with high accuracy. In the UltraSPARC **prefetch** and dispatch unit design, we examined a technique that combined two prediction methods: predictive set...

...prediction. This combination was compared with alternative designs such as direct-mapped and set-associative **caches** , and a branch **history** table and a branch target buffer. We chose the combined prediction technique for its fast...

...This paper summarizes the trade-off decisions made in the design of the UltraSPARC instruction **prefetch** and dispatch unit. (Author abstract) 22 Refs.
Identifiers: UltraSPARC instruction **prefetch** architecture

21/3,K/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01959581 E.I. Monthly No: EI8604028582 E.I. Yearly No: EI86031147
Title: PREFETCHING **USING A PAGEABLE BRANCH HISTORY TABLE.**
Author: Anon
Source: IBM Technical Disclosure Bulletin v 28 n 8 Jan 1986 p 3510-3511
Publication Year: 1986
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH

Title: PREFETCHING **USING A PAGEABLE BRANCH HISTORY TABLE.**
Abstract: **Prefetching** of cache lines using a pageable branch history table (PBHT) improves machine performance through better...
Identifiers: **PREFETCHING** ; PAGEABLE BRANCH **HISTORY** TABLE; **CACHE** LINES; **CACHE** MISS RATIO; PROBABLE RESOLUTION

21/3,K/7 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01594643 ORDER NO: AADMM-19345
HISTORY GUIDED PREFETCHING **IN A TELEPHONE SWITCHING APPLICATION**
Author: EL EBIARY, MOHAMED HATEM
Degree: M.A.SC.
Year: 1994
Corporate Source/Institution: UNIVERSITY OF TORONTO (CANADA) (0779)
Source: VOLUME 35/06 of MASTERS ABSTRACTS.
PAGE 1855. 182 PAGES
ISBN: 0-612-19345-4

HISTORY GUIDED PREFETCHING **IN A TELEPHONE SWITCHING APPLICATION**

...delay gap between the fast processor and the slow main memory.
This research proposes a **prefetch** strategy that is guided by the program's **cache** miss **history** . This **prefetch** strategy is used to improve the performance of a RISC-based system used by Bell...

21/3,K/8 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

01106966 INSIDE CONFERENCE ITEM ID: CN010844319
A Miss History **-Based Architecture for** Cache Prefetching
Phalke, V.; Gopinath, B.
CONFERENCE: Memory management-International workshop
LECTURE NOTES IN COMPUTER SCIENCE, 1995; ISSUE 986 P: 381-398
Berlin, New York, Springer, c1995
ISSN: 0302-9743 ISBN: 3540603689
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE EDITOR(S): Baker, H. G.
CONFERENCE LOCATION: Kinross
CONFERENCE DATE: Sep 1995 (199509) (199509)
NOTE:
Also known as IWMM '95

A Miss History **-Based Architecture for** Cache Prefetching

21/3,K/9 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

8017566 INSPEC Abstract Number: C2004-08-6120-021
Title: Call graph prefetching **for database applications**
Author(s): Murali Annavaram; Patel, J.M.; Davidson, E.S.
Author Affiliation: Intel Corp., Santa Clara, CA, USA
Journal: ACM Transactions on Computer Systems vol.21, no.4 p.412-44
Publisher: ACM,
Publication Date: Nov. 2003 Country of Publication: USA
CODEN: ACSYEC ISSN: 0734-2071
SICI: 0734-2071(200311)21:4L.412:CGPD;1-#
Material Identity Number: E606-2003-004
U.S. Copyright Clearance Center Code: 0734-2071/03/1100-0412$5.00
Language: English
Subfile: C

Title: Call graph prefetching **for database applications**
...Abstract: and data footprints and hence do not use processor caches effectively. We propose Call Graph **Prefetching** (CGP), an N instruction **prefetching** technique that analyzes the call graph of a database system and **prefetches** instructions from the function that is deemed likely to be called next. CGP capitalizes on...
... and uses the predictable call sequences in the call graph to determine which function to **prefetch** next. The hardware-based CGP(CGP...

...H) uses a hardware table, called the Call Graph **History Cache** (CGHC), to dynamically store sequences of functions invoked during program execution, and uses that stored history when choosing which functions to **prefetch** . We evaluate the performance of CGP on sets of Wisconsin and TPC-H queries, as...

... applications the number of instruction cache (I-cache) misses were very few even without any **prefetching** , obviating the need for CGP. On the other hand, the database workloads do suffer a...
Identifiers: call graph **prefetching** ; ...

...N instruction **prefetching** technique...

...Call Graph **History Cache** hardware table

21/3,K/10 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4643568 INSPEC Abstract Number: C9405-6120-040
Title: A page prefetching **mechanism based on repeated memory access patterns**
Author(s): Inshik Song; Sanglyul Min; Yookun Cho
Journal: Journal of the Korea Information Science Society vol.20, no.12 p.1842-51
Publication Date: Dec. 1993 Country of Publication: South Korea
CODEN: HJKHDC ISSN: 0258-9125
Language: Korean

Subfile: C

Title: A page prefetching **mechanism based on repeated memory access patterns**

...Abstract: programs exhibit repeated memory access patterns. Assuming such memory access patterns, we propose a page **prefetching** mechanism to reduce page-in delay time. We gather page fault information into **history buffer** at run time. In case that a given page has been faulty more than once, pager **prefetches** the next page faulted following that page in the past. Using only 1-2 % of total free page frames for page fault **history buffers** and **prefetch buffers** , we observed high **prefetch** hit-ratio of about 50 % among all page faults. This historical page **prefetching** reduces page-in delay by about 20%. This mechanism may be useful in demand-paging...

Identifiers: page **prefetching** mechanism...

21/3,K/11 (Item 3 from file: 2)

4585171 INSPEC Abstract Number: C9403-6150J-049

Title: Page prefetching **based on fault history**

Author(s): Inshik Song; Yookun Cho

Author Affiliation: Dept. of Comput. Eng., Seoul Nat. Univ., South Korea

Conference Title: Proceedings of the USENIX Mach III Symposium p. 203-13

Publisher: USENIX Assoc, Berkeley, CA, USA

Publication Date: 1993 Country of Publication: USA 322 pp.

Material Identity Number: XX93-00527

Conference Date: 19-21 April 1993 Conference Location: Santa Fe, NM, USA

Language: English

Subfile: C

Title: Page prefetching **based on fault history**

...Abstract: programs exhibit repeated memory access patterns. Assuming this memory access behavior, we propose a page **prefetching** method to reduce page-in delay time. We gather page fault information into a **history buffer** at run time. If a page fault occurs more than once for a given page, the pager **prefetches** the next page faulted following that page in the history. Using only 1% of the total free page frames for page fault **history** and page **prefetch buffers** , we have observed a high fault-again ratio of about 70% and a **prefetch** hit ratio of about 50% across all page faults. This historical page **prefetching** reduces page-in delay and increases paging performance by 20%. This method may be useful...

Identifiers: page **prefetching** ; ...

... **history buffer** ;

21/3,K/12 (Item 4 from file: 2)

01614759 INSPEC Abstract Number: C81001767

Title: Using a Branch History **Table to** prefetch cache **lines**
Author(s): Rechtschaffen, R.N.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.22, no.12 p.5539
Publication Date: May 1980 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Subfile: C

Title: Using a Branch History **Table to** prefetch cache **lines**
Abstract: A Branch **History** Table (BHT) issues **cache** accesses independently of the decoding of instructions or the availability of instructions at the processor. In particular, should a branch target miss in the cache, the next miss **prefetch** can be derived from the Branch History Table through its normal operation. This method establishes...

... provides the basis for the above. The Branch History Table need not be used to **prefetch** instructions but merely to manage the instruction portion of the cache in case of a...
...Identifiers: cache line **prefetching** ;

```
File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
File 347:JAPIO Nov 1976-2004/May(Updated 040903)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200461
         (c) 2004  Thomson Derwent

Set     Items   Description
S1        261   HISTOR??(3N)(BUFFER?? OR CACHE?? OR TEMPORARY??(2N)STORAG?-
            ??)
S2     400015   FLAG?? OR BIT OR BITS OR INDICATOR??
S3      49222   (MEMOR???? OR STORAGE??? OR RAM? ?)(2N)(LOCATION?? OR ADDR-
            ESS??)
S4       2436   (SECOND??? OR 2ND?? OR NEXT?? OR SUBSEQUENT???)(4N)S3
S5      14236   (PRE()(FETCH??? OR READ??? OR LOAD???) OR PREFETCH??? OR P-
            RELOAD??? OR PREREAD???)
S6       2764   STRIDE??? OR STRIDING??
S7    1260781   INTERVAL?? OR GAP?? OR DISTANC??
S8         49   S1 AND S2
S9          0   S8 AND S4
S10         7   S8 AND S3
S11         3   S10 AND S5
S12         1   S8 AND S6
S13         1   S12 NOT S11
S14         0   S8 AND S7
S15         3   S1 AND S4
S16         3   S15 NOT (S11 OR S12)
```

11/5/1 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

016169895 **Image available**
WPI Acc No: 2004-327782/200430
Related WPI Acc No: 2003-874452
XRPX Acc No: N04-261484

Computer system has pre - fetcher **which** pre - fetches **data associated with specified** memory location **from** memory , **if no** flag **associated with specified** memory location **is in request** history buffer

Patent Assignee: BOGIN Z (BOGI-I); HUM H H (HUMH-I)
Inventor: BOGIN Z; HUM H H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040059873	A1	20040325	US 2000541392	A	20000331	200430 B
			US 2003628434	A	20030729	

Priority Applications (No Type Date): US 2000541392 A 20000331; US 2003628434 A 20030729
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040059873	A1		21	G06F-012/08	Cont of application US 2000541392 Cont of patent US 6643743

Abstract (Basic): US 20040059873 A1

NOVELTY - A **prefetch** control unit checks the request **history buffer** (RHB) for **flag** associated with specified **memory location** that is based on previous **memory location** called by processor. A **pre - fetcher pre - fetches** data associated with the specified **memory location** from **memory** , if no **flag** associated with the specified **memory location** is in the RHB.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an apparatus for **pre - fetching** data

USE - Computer system performing streaming-down **prefetch** of data into cache memory. Also, the streaming-down **prefetch** is applicable for programmable gate array device, application specific integrated circuit (ASIC).

ADVANTAGE - Lowers the cold-start miss rate by examining the history of data requests, anticipating which data will be requested and **prefetching** that data while decreasing the overall number of cache misses.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the **prefetch** cache.

prefetch cache (2)
data field (4)
tag (6)
pp; 21 DwgNo 1/7

Title Terms: COMPUTER; SYSTEM; PRE; PRE; DATA; ASSOCIATE; SPECIFIED; MEMORY ; LOCATE; MEMORY; NO; **FLAG** ; ASSOCIATE; SPECIFIED; MEMORY; LOCATE; REQUEST; HISTORY; BUFFER
Derwent Class: T01; U14
International Patent Class (Main): G06F-012/08
File Segment: EPI

11/5/2 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

015812248 **Image available**
WPI Acc No: 2003-874452/200381
Related WPI Acc No: 2004-327782
XRPX Acc No: N03-698165
Data prefetching **method in cache, involves storing** flag **in response to fetching of data from memory, in request** history buffer **for further data access**
Patent Assignee: INTEL CORP (ITLC)
Inventor: BOGIN Z; HUM H H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6643743	B1	20031104	US 2000541392	A	20000331	200381	B

Priority Applications (No Type Date): US 2000541392 A 20000331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6643743	B1		12	G06F-012/00	

Abstract (Basic): US 6643743 B1
NOVELTY - The method involves fetching data from a memory according to a request from a **memory address** . A **flag** is stored in response to fetching process, in a request **history buffer** (RHB) (8). Another data is **prefetched** from another **memory address** , when data from the another **memory address** is not flagged in the RHB.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer system.
USE - For **prefetching** data in cache used in programmable gateway devices, application specific integrated circuits (ASIC).
ADVANTAGE - Efficiently **prefetches** data and accurately anticipates spatial locality.
DESCRIPTION OF DRAWING(S) - The figure shows out-of-order stream-up data access trend in cache.
prefetch cache (2)
request **history buffer** (8)
data fields (10,12)
pp; 12 DwgNo 4C/7
Title Terms: DATA; METHOD; CACHE; STORAGE; **FLAG** ; RESPOND; FETCH; DATA; MEMORY; REQUEST; HISTORY; BUFFER; DATA; ACCESS
Derwent Class: T01
International Patent Class (Main): G06F-012/00
File Segment: EPI

11/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

010188295 **Image available**
WPI Acc No: 1995-089549/199512
XRPX Acc No: N95-070819
History buffer **- has FIFOs located in memory controller, with system storing addresses for read requests made by CPU, and if next sequential address is detected in subsequent read request, this is designated to be stream of sequential reads**

Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: GOODWIN P M; MASKAS B A; THALLER K M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5388247	A	19950207	US 9337247	A	19930514	199512 B
			US 94197376	A	19940216	

Priority Applications (No Type Date): US 94197376 A 19940216; US 9337247 A 19930514
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5388247	A		25	G06F-011/34	CIP of application US 9337247

Abstract (Basic): US 5388247 A

The read buffering system uses a bank of FIFOs to hold sequential read data for a number of data streams being fetched by a computer. The FIFOs are located in the memory controller, so the system bus is not used in memory accesses used to fill the stream buffer. The system stores addresses for read requests made by a CPU, and if a next sequential address is then detected in a subsequent read request, this is designated to be a stream (i.e., sequential reads).

When a stream is thus detected, data is fetched from DRAM **memory** for **addresses** following the sequential address, and this **prefetched** data is stored in one of the FIFOs.

The unnecessary **prefetching** of data is prevented by stopping certain CPU requests from being used to detect streams. A FIFO is selected using a least-recently-used algorithm. When the CPU subsequently makes a read request for data in a FIFO, this data can be returned without making a memory access. By taking advantage of page mode, access to the DRAM memory for the **prefetch** operations can be transparent to the CPU, resulting in performance improvement if sequential accesses are frequent. The data is stored in the DRAMs with ECC check **bits** , and error detection and correction (EDC) is performed on the read data downstream of the stream buffer, so the stream buffer is protected by EDC.

Dwg.5/15

Title Terms: HISTORY; BUFFER; LOCATE; MEMORY; CONTROL; SYSTEM; STORAGE; ADDRESS; READ; REQUEST; MADE; CPU; SEQUENCE; ADDRESS; DETECT; SUBSEQUENT; READ; REQUEST; DESIGNATED; STREAM; SEQUENCE; READ
Derwent Class: T01
International Patent Class (Main): G06F-011/34
File Segment: EPI
?

13/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010845641 **Image available**
WPI Acc No: 1996-342594/199635
XRPX Acc No: N96-288356

Filtered stream buffer for pre-fetching data from memory for vector processing computer - has filtered stream buffer comprising cache block storage area and filter controller for determining if second address has set relationship to 1st address, to pre-fetch stream data into cache block storage area

Patent Assignee: CRAY RES INC (CRAY)
Inventor: KESSLER R E; OBERLIN S M; PALACHARLA S; SCOTT S L

Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CA 2146489	A	19960502	CA 2146489	A	19950406	199635	B
US 5761706	A	19980602	US 94333133	A	19941101	199829	

Priority Applications (No Type Date): US 94333133 A 19941101
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CA 2146489	A		65	G06F-013/20	
US 5761706	A			G06F-012/00	

Abstract (Basic): CA 2146489 A

A filtered stream buffer includes a cache block storage area and a filter controller. The filter controller determines whether a pattern of references has a predetermined relationship, and if so, pre-fetches stream data into the cache block storage area.

The filtered stream **buffer** includes a **history** table, a validity **indicator** which is associated with the cache block storage area and indicates which cache blocks, if any, are valid. Alternatively, the filtered stream buffer controls random access memory (RAM) chips to stream the consecutive cache blocks from the RAM into the cache block storage area. **Strided** cache blocks, each correspond to an address determined by adding to the first address, an integer multiple of the difference between the second address and the first address.

The processor generates three addresses of data words in the memory, and the filter controller determines whether a predetermined relationship exists among the three addresses, and if so, pre-fetches **stride** stream data into the cache block storage area.

USE/ADVANTAGE - In vector processing computer, where once processor starts to fetch vector, addresses of future fetches can be predicted based in pattern of past fetches. Reduced memory bandwidth requirement of stream buffer. High hit rates comparable to local hit rates of very large caches. Successfully detects programs that have high percentage of non-unit **stride** references.

Dwg.3A/18

Title Terms: FILTER; STREAM; BUFFER; PRE; FETCH; DATA; MEMORY; VECTOR; PROCESS; COMPUTER; FILTER; STREAM; BUFFER; COMPRISE; CACHE; BLOCK;

STORAGE; AREA; FILTER; CONTROL; DETERMINE; SECOND; ADDRESS; SET; RELATED; ADDRESS; PRE; FETCH; STREAM; DATA; CACHE; BLOCK; STORAGE; AREA

Derwent Class: T01

International Patent Class (Main): G06F-012/00; G06F-013/20

File Segment: EPI

16/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014050105 **Image available**
WPI Acc No: 2001-534318/200159
Cache system
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM M J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001026920	A	20010406	KR 9938427	A	19990909	200159	B

Priority Applications (No Type Date): KR 9938427 A 19990909
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001026920	A		1	G06F-012/08	

Abstract (Basic): KR 2001026920 A
NOVELTY - The cache system is provided to improve the hit ratio of the cache memory.
DETAILED DESCRIPTION - The cache system(100) comprises the tag memory(20), the data memory (30), the first address register(10), the second address register(40), the adjacent block discrimination part(50), the **cache** access **history** table(CHT,60), the comparator(70), and the controller(80). The cache system temporarily stores the data between the CPU and the main memory. The first address register stores the current access address of the tag and data **memory**. The **second address** register stores the late access address of the tag and data memory. The adjacent block discrimination part checks if the hit/miss about the access of the tag memory is or not, and generates the discrimination signal responding to the adjacent relationship between two addresses. The CHT stores the access state of the tag and data memory. When the access about the tag memory hits, the controller reads the data from the data memory and offers the data to the CPU. When the access about the tag memory misses, the first or the second block is loaded from the main memory to the data memory and the access state of the tag and data memory is stored in the CHT.
pp; 1 DwgNo 1/10
Title Terms: CACHE; SYSTEM
Derwent Class: T01
International Patent Class (Main): G06F-012/08
File Segment: EPI

16/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011073610 **Image available**
WPI Acc No: 1997-051534/199705
XRPX Acc No: N97-042426
Memory stream buffer - receiving 2nd **read command specifying** 2nd memory address **sequentially following 1st, fetching data from address following 2nd address if 1st read and write addresses are different, otherwise not fetching**
Patent Assignee: DIGITAL EQUIP CORP (DIGI)

Inventor: GOODWIN P M; THALLER K M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5586294	A	19961217	US 9337240	A	19930326	199705	B
			US 94197368	A	19940216		

Priority Applications (No Type Date): US 94197368 A 19940216; US 9337240 A 19930326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5586294	A		26	G06F-013/00	CIP of application US 9337240

Abstract (Basic): US 5586294 A

The read buffering system employs FIFOs to hold sequential read data for a number of data streams being fetched by a computer. When the system sees a read command from the CPU, it stores an incremented value of the address of the read command in a **history buffer** and marks the entry as valid. The system detects a stream when a subsequent read command specifies an address that matches the address value stored in the **history buffer** .

Upon detecting a stream, the system fetches data from DRAMs at addresses that follow the address of the subsequent read command, and stores it in a FIFO. However, to reduce unnecessary pre-fetching, the system looks for a read X, write X, read X+1 (where X and X+1 designate addresses) succession of commands to prevent them from creating a stream. This succession occurs often and qualifies as a stream, but is seldom followed by other reads that maintain the stream. The system checks for this succession by comparing an incremented value of the address of the write command with each valid address value stored in the **history buffer** . A match causes the system to invalidate the **history buffer** entry containing the matched address value. This effectively disables the use of this address value for detecting a stream upon subsequent read commands and, consequently, for pre-fetching data from memory.

ADVANTAGE - Performance improvement.

Dwg.5/15

Title Terms: MEMORY; STREAM; BUFFER; RECEIVE; READ; COMMAND; SPECIFIED; MEMORY; ADDRESS; SEQUENCE; FOLLOW; FETCH; DATA; ADDRESS; FOLLOW; ADDRESS; READ; WRITING; ADDRESS; FETCH
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

16/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010325517 **Image available**
WPI Acc No: 1995-226791/199530
XRPX Acc No: N95-177733

Compressing and decompressing sequential data - using received data element as address to location in memory and determines whether addressed memory location contains first record of first matching data element, generates pointer to data element

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: STROHACKER O C
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 660531	A2	19950628	EP 94308515	A	19941117	199530	B
CA 2132762	A	19950624	CA 2132762	A	19940923	199538	
JP 7200247	A	19950804	JP 94246548	A	19941012	199540	
EP 660531	A3	19960207	EP 94308515	A	19941117	199622	
US 5563595	A	19961008	US 93173738	A	19931223	199646	
CA 2132762	C	19991109	CA 2132762	A	19940923	200013	

Priority Applications (No Type Date): US 93173738 A 19931223
Cited Patents: No-SR.Pub; EP 380294; US 5150430
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 660531	A2	E	17	H03M-007/30	
Designated States (Regional): DE FR GB					
CA 2132762	C	E		H03M-007/30	
JP 7200247	A		12	G06F-005/00	
US 5563595	A		16	H03M-007/30	
CA 2132762	A			H03M-007/30	
EP 660531	A3			H03M-007/30	

Abstract (Basic): EP 660531 A

The apparatus uses received data element as an address to a location in memory and determines whether the addressed memory location contains a first matching data element and generates a pointer to the first matching data element. A second received data element is received as a **second** address to a **second location** in the **memory** .

It is determined whether the **second** addressed **location** of the **memory** includes a **second** matching data element contiguous to the first matching data element.The received data element is used as an address to one of several shift registers. A data processing system includes a memory for storing data, a processor for processing the data, and a data compressor.

ADVANTAGE - Compression is more effective than many existing Lempel-Ziv techniques because search for matching data strings is exhaustive, while **history buffer** allows for exhaustive search for all possible matching strings.

Dwg.4/6

Title Terms: COMPRESS; DECOMPRESS; SEQUENCE; DATA; RECEIVE; DATA; ELEMENT; ADDRESS; LOCATE; MEMORY; DETERMINE; ADDRESS; MEMORY; LOCATE; CONTAIN; FIRST; RECORD; FIRST; MATCH; DATA; ELEMENT; GENERATE; POINT; DATA; ELEMENT
Derwent Class: T01; U21
International Patent Class (Main): G06F-005/00; H03M-007/30
International Patent Class (Additional): G06F-013/16; H03M-007/40; H03M-007/46
File Segment: EPI

File 9:Business & Industry(R) Jul/1994-2004/Sep 24
(c) 2004 The Gale Group
File 15:ABI/Inform(R) 1971-2004/Sep 27
(c) 2004 ProQuest Info&Learning
File 16:Gale Group PROMT(R) 1990-2004/Sep 27
(c) 2004 The Gale Group
File 20:Dialog Global Reporter 1997-2004/Sep 27
(c) 2004 The Dialog Corp.
File 47:Gale Group Magazine DB(TM) 1959-2004/Sep 27
(c) 2004 The Gale group
File 75:TGG Management Contents(R) 86-2004/Sep W3
(c) 2004 The Gale Group
File 80:TGG Aerospace/Def.Mkts(R) 1986-2004/Sep 27
(c) 2004 The Gale Group
File 88:Gale Group Business A.R.T.S. 1976-2004/Sep 24
(c) 2004 The Gale Group
File 112:UBM Industry News 1998-2004/Jan 27
(c) 2004 United Business Media
File 141:Readers Guide 1983-2004/Aug
(c) 2004 The HW Wilson Co
File 148:Gale Group Trade & Industry DB 1976-2004/Sep 27
(c)2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2004/Sep 27
(c) 2004 The Gale Group
File 264:DIALOG Defense Newsletters 1989-2004/Sep 27
(c) 2004 The Dialog Corp.
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 484:Periodical Abs Plustext 1986-2004/Sep W3
(c) 2004 ProQuest
File 553:Wilson Bus. Abs. FullText 1982-2004/Aug
(c) 2004 The HW Wilson Co
File 570:Gale Group MARS(R) 1984-2004/Sep 27
(c) 2004 The Gale Group
File 608:KR/T Bus.News. 1992-2004/Sep 27
(c)2004 Knight Ridder/Tribune Bus News
File 620:EIU:Viewswire 2004/Sep 17
(c) 2004 Economist Intelligence Unit
File 613:PR Newswire 1999-2004/Sep 27
(c) 2004 PR Newswire Association Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Sep 27
(c) 2004 The Gale Group
File 623:Business Week 1985-2004/Sep 20
(c) 2004 The McGraw-Hill Companies Inc
File 624:McGraw-Hill Publications 1985-2004/Sep 20
(c) 2004 McGraw-Hill Co. Inc
File 634:San Jose Mercury Jun 1985-2004/Sep 25
(c) 2004 San Jose Mercury News
File 635:Business Dateline(R) 1985-2004/Sep 25
(c) 2004 ProQuest Info&Learning
File 636:Gale Group Newsletter DB(TM) 1987-2004/Sep 27
(c) 2004 The Gale Group
File 647:CMP Computer Fulltext 1988-2004/Sep W3
(c) 2004 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2004/Sep 27
(c) 2004 The Dialog Corp.
File 674:Computer News Fulltext 1989-2004/Aug W4
(c) 2004 IDG Communications

File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc

Set	Items	Description
S1	1364	HISTOR??(3N)(BUFFER?? OR CACHE?? OR TEMPORARY??(2N)STORAG?-??)
S2	4936523	FLAG?? OR BIT OR BITS OR INDICATOR??
S3	41830	(MEMOR???? OR STORAGE??? OR RAM? ?)(2N)(LOCATION?? OR ADDRESS??)
S4	558	(SECOND??? OR 2ND?? OR NEXT?? OR SUBSEQUENT???)(4N)S3
S5	47209	(PRE()(FETCH??? OR READ??? OR LOAD???) OR PREFETCH??? OR PRELOAD??? OR PREREAD???)
S6	317265	STRIDE??? OR STRIDING??
S7	3342460	INTERVAL?? OR GAP?? OR DISTANC??
S8	0	S1(S)S4
S9	48	S1(S)S2
S10	16	S1(S)S5
S11	0	S9 AND S10
S12	3	S10 AND S3
S13	6	S9 AND S3
S14	4	RD (unique items)
S15	4	S14 NOT S12
S16	0	S1(S)S6
S17	7	S1 AND S6
S18	3	RD (unique items)
S19	1	S18 AND S3
S20	0	S19 NOT (S15 OR S12)
S21	36	S1(S)S7
S22	0	S21(S)S3

12/3,K/1 (Item 1 from file: 88)
DIALOG(R)File 88:Gale Group Business A.R.T.S.

05683201 SUPPLIER NUMBER: 70870222
Data Prefetch Mechanisms.
VANDERWIEL, STEVEN P.; LILJA, DAVID J.
ACM Computing Surveys, 32, 2, 174
June, 2000
ISSN: 0360-0300 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 13031 LINE COUNT: 01071

... this implies either maintaining (Delta) address registers to hold multiple prefetch addresses or storing these **addresses** in **memory** if the required number of registers is not available.

Comparing the transformed loop in Figure...requirements were found to increase sharply as a result of the large number of unnecessary **prefetches** generated by the stream buffers. To help mitigate this effect, a small **history buffer** is used to record the most recent primary **cache** misses. When this **history buffer** indicates that misses have occurred for both block b and block b + 1, a stream is allocated and blocks b + 2, ..., b + K + 1 are **prefetched** into the buffer. Using this more selective stream allocation policy, bandwidth requirements were reduced at...

...instructions. The organization of the RPT is given in Figure 8. Table entries contain the **address** of the **memory** instruction, the previous address accessed by this instruction, a stride value for those entries that ...an integrated technique that enables prefetching for irregular data structures. This is accomplished by tagging **memory locations** in such a way that a reference to one element of a data object initiates...

12/3,K/2 (Item 1 from file: 112)
DIALOG(R)File 112:UBM Industry News

01126906 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Motorola's ColdFire V3 boosts multimedia designs
What's new in Electronics Europe , p 19
March, 1998
LANGUAGE: English RECORD TYPE: Fulltext DOC. TYPE: Journal
WORD COUNT: 00002024

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...placement of the instruction decode in the processor's pipelines.

The single-cycle K-bus **memory** access was **addressed** by dividing it into a two-stage pipelined process.

The first K-bus access cycle...table is implemented. Control information allows the branches to be `predicted', based on past execution **history** .

Unlike a branch **cache** , the change-of-flow acceleration technique in the V3 design applies to all branches as they are **prefetched** , and it is not limited by the size of a branch **cache** or past execution **history** . Ultimately, this approach provides a substantial improvement in branch execution time.

The V3 core employs...

12/3,K/3 (Item 1 from file: 484)

04978447 SUPPLIER NUMBER: 68546547 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Data prefetch mechanisms
Vanderwiel, Steven P; Lilja, David J
ACM Computing Surveys (ACI), v32 n2, p174-199, p.26
Jun 2000
ISSN: 0360-0300 JOURNAL CODE: ACI
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 12304

TEXT:
... this implies either maintaining 8 address registers to hold multiple prefetch addresses or storing these **addresses** in **memory** if the required number of registers is not available.

Comparing the transformed loop in Figure...requirements were found to increase sharply as a result of the large number of unnecessary **prefetches** generated by the stream buffers. To help mitigate this effect, a small **history buffer** is used to record the most recent primary **cache** misses. When this **history buffer** indicates that misses have occurred for both block b and block b + 1, a stream is allocated and blocks b + 2, ..., b + K + 1 are **prefetched** into the buffer. Using this more selective stream allocation policy, bandwidth requirements were reduced at...

...instructions. The organization of the RPT is given in Figure 8. Table entries contain the **address** of the **memory** instruction, the previous address accessed by this instruction, a stride value for those entries that ...an integrated technique that enables prefetching for irregular data structures. This is accomplished by tagging **memory locations** in such a way that a reference to one element of a data object initiates...
?

15/3,K/1 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

07877634 SUPPLIER NUMBER: 16882233 (USE FORMAT 7 OR 9 FOR FULL TEXT)
New algorithm improves branch prediction; better accuracy required for highly superscalar designs. (includes related article on the taxonomy of Tse-Yu Yeh's and Yale Patt's algorithm) (Technical)
Gwennap, Linley
Microprocessor Report, v9, n4, p17(5)
March 27, 1995
DOCUMENT TYPE: Technical ISSN: 0899-9341 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 3963 LINE COUNT: 00314

... instruction cache, for example, one per every four instructions. When instructions are fetched from the **cache** , the **history bit** comes along. If the **bit** is set, that group of instructions contains a predicted-taken branch, and the fetch stream...of a register to determine their destination. To handle these instructions, some processors use special **storage** for return **addresses** .

When a subroutine is called, processors such as Cyrix's M1 and all Alpha chips...each BTB entry also contains a 24-bit tag and a 32-bit predicted target **address** , this added **storage** requirement would not be onerous. With such a small [kappa] value, there is little need...

15/3,K/2 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

03323771 SUPPLIER NUMBER: 06041877 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Focus on dense DSP ICs that match supermini speed. (digital signal processors)
Leonard, Milt
Electronic Design, v35, p131(7)
Oct 15, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4391 LINE COUNT: 00333

... an added data access, resulting in two data accesses during one cycle. In operation, the **cache** keeps a small **history** of previously executed instructions. When a program enters a loop, which usually contains time-critical...

...by 16 bits of external memory can be directly addressed by the 14-bit data- **memory address** bus. The program memory bus, also 14 bits wide, can directly address up to 32k...bit data RAMs, and I/O access to two 64k-by-22-bit external data- **memory address** spaces. Each data **memory** has an **address** generator. The arithmetic unit is programmable for either 22-bit floating-point or 16-bit...link directly with 8- and 16-bit microprocessors.

Photo: 1. Using external program and data **memory address** spaces in a Harvard architecture, Analog Devices' 16-bit ADSP2100 digital signal processor executes two...
CAPTIONS: Using external program and data **memory address** spaces in a Harvard architec. (chart); To maintain 16-point resolution for a 32-bit...

15/3,K/3 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01773712 SUPPLIER NUMBER: 16839484 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Nx586 battles P5. (NexGen Nx586, Pentium P5 processors) (Post-Pentium x86 Chips beat the Clock)
Case, Brian
Windows Sources, v3, n5, p163(2)
May, 1995
ISSN: 1065-9641 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1238 LINE COUNT: 00097

...ABSTRACT: into more simple internal operations using a 24-byte prefetch buffer. The processor includes an **address / memory** reference unit, a full integer unit and a simple integer execution unit, which accepts only...
... internal operations, which NexGen calls RISC86 instructions. The chip employs three RISC86 execution units: an **address / memory** -reference unit; a simple integer-execution unit, which accepts only single-cycle ALU operations; and...

...at the predicted branch target and the target address, and a 2,048-entry branch **history cache** . This secondary **cache** is four times as big as the P6's, but it uses 2- **bit** prediction instead of the P6's 4. If the primary cache hits, the decoder can...

15/3,K/4 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2004 CMP Media, LLC. All rts. reserv.

00557305 CMP ACCESSION NUMBER: EET19900528S0873
Tools for 8-bit microcontroller design get smart
RICHARD GOERING
ELECTRONIC ENGINEERING TIMES, 1990, n 592, 29
PUBLICATION DATE: 900528
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: DES
WORD COUNT: 2479

... a different approach by allocating all data statically, placing functional parameters and variables into fixed- **memory locations** . This new compiler claims ANSI C compatibility with code that's 50 percent more compact...trace buffer without stopping emulation."
HMI offers such a capability by dividing its 8k 88- **bit** trace buffer into two 4k 88- **bit** buffers. A "break" **buffer** provides a trace **history** that terminates with an emulation break, while a "trigger" buffer uses an independent trigger point...
?